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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,096	11/03/2003	Jin Tak Kim	CU-3423 RJS	2817

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LADAS & PARRY LLP
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CHICAGO, IL 60604

EXAMINER

PERVAN, MICHAEL

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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07/12/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/700,096

Applicant(s)

KIM ET AL.

Examiner

Michael Pervan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 November 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>5/3/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Yamazaki et al (JP 05-035202; machine translation provided) in further view of Iinuma (US 2001/0043203).

In regards to claim 1, the APA discloses (Figure 1) a device for adjusting control signals for an LCD, comprising:

an LCD module (100) having an LCD panel (106) for displaying a picture, a timing controller (110) for adjusting a data supply and a driving signal (pg. 1, line 24- pg.2, line 3), a voltage generating unit (112) for generating a driving voltage (pg. 2, lines 3-5) and an input unit (116) provided with a plurality of control signal pins which are adjusted by an external adjustment signal (pg. 1, lines 15-21; the input unit receives signals from the outside (external) that control (adjust) the above units, namely LCD panel, timing controller, voltage generating unit and a control signal generating unit, therefore it has a plurality of control signals that are adjusted by an external adjustment signal); and

a conversion board device (200) having a scaler unit (202) for generating and providing data (pg. 2, lines 9-11) and a power supply required for the LCD module and a

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power supply unit (204) (pg. 2, lines 11-13), said scaler unit digitizing inputs to the LCD module and scaling said inputs signals to the LCD module to match the LCD module (pg. 2, lines 9-11).

The APA does not disclose the conversion board device generating and outputting a pulse width modulation (PWM) signal to a voltage generating unit of the LCD module, the PWM signal being provided to the LCD module as a common voltage, the PWM signal having an amplitude that does not vary, wherein the scaler is provided with microcomputer GPIO ports, and the microcomputer GPIO ports control the plurality of control signal pins provided in the input unit.

Yamazaki discloses the conversion board device generating and outputting a pulse width modulation (PWM) signal to a voltage generating unit of the LCD module, the PWM signal being provided to the LCD module as a common voltage, the PWM signal having an amplitude that does not vary (paragraphs 7-11).

It would have been obvious at the time of invention to modify the APA and linuma by incorporating Yamazaki, PWM signal provided to LCD as a common voltage and having an amplitude that does not vary, because it improves performance of gradation displays.

APA and Yamazaki do not disclose wherein the scaler is provided with microcomputer GPIO ports, and the microcomputer GPIO ports control the plurality of control signal pins provided in the input unit.

linuma discloses microcomputer GPIO ports (paragraph 56; Graphic controller is outside the display and has GPIO terminal).

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It would have been obvious at the time of invention to modify the APA and Yamazaki by incorporating the teachings of linuma, a graphic controller, provided with a GPIO terminal, is connected to an IO terminal of a flat panel controller, by adding the graphic controller of linuma to the scaler unit of the APA and Yamazaki because GPIO devices provide a set of IO ports which can be configured for either input or output, support for common bus protocols like I²C, SPI and SMBus serial buses are cheaper than using a microcontroller.

In regards to claim 2, the APA, Yamazaki and linuma disclose the plurality of control signal pins are for signals of FRC_EN, TDDI, LVDS_MAP_SEL, and the signals are properly adjusted under the control of the microcomputer GPIO ports to be transferred to the controller (pg. 1, lines 15-21; since the input unit receives signals from the GPIO terminal of the scaler unit to control the above units, namely LCD panel, timing controller, voltage generating unit and a control signal generating unit, and the control signal generating unit generates FRC_Enable, LVDS_MAP_SEL and TDDI signals, therefore the control FRC_Enable, LVDS_MAP_SEL and TDDI signals are properly adjusted by GPIO ports).

Response to Arguments

3. Applicant's arguments with respect to claims 1-2 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art (Park US 6,816,139) is deemed relevant since it discusses control signals being external to the LCD panel.
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MVP
July 5, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

